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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,476	04/22/2004	Yoshihisa Nagano	740819-1052	5876
22204	7590	04/06/2007		
NIXON PEABODY, LLP 401 9TH STREET, NW SUITE 900 WASHINGTON, DC 20004-2128			EXAMINER WILSON, SCOTT R	
			ART UNIT	PAPER NUMBER
			2826	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/06/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/829,476	Applicant(s) NAGANO ET AL.	
	Examiner Scott R. Wilson	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 April 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>See Continuation Sheet</u> . | 6) <input type="checkbox"/> Other: _____ |

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :4/22/04, 8/11/04,9/17/04, 7/28/05.

DETAILED ACTION

Reissue Applications

The reissue oath/declaration filed with this application is defective because it fails to identify at least one error which is relied upon to support the reissue application. See 37 CFR 1.175(a)(1) and MPEP § 1414. The reason why the deletions of claim 1 correct an error or errors is unclear.

Claims 1-7 are rejected as being based upon a defective reissue oath under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the oath is set forth in the discussion above in this Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al. in view of Evans, Jr.. Izumi et al., Figure 9, discloses (col. 13, lines 34-53) a semiconductor device comprising: a protective insulating film (10) deposited on a semiconductor substrate (1) having first (5) and second (12) field-effect transistors formed thereon; a capacitor (6) composed of a capacitor lower electrode (7), a capacitor insulating film (8) made of an insulating metal oxide (col. 6, lines 34-36), and a capacitor upper electrode (9) which are formed in upwardly stacked relationship on the protective insulating film; a first contact plug, embodied as the thickness of the lower capacitor electrode, formed in the protective insulating film to provide a connection between an impurity diffusion layer (2) serving as a source or drain region of the first field-effect transistor and the capacitor lower electrode, and a second contact plug, embodied as the thickness of the wiring line (11), formed in the protective insulating film to provide a connection between an impurity diffusion layer (25) serving as a source or drain region of the second

Art Unit: 2826

field-effect transistor and the capacitor upper electrode. The capacitor upper electrode (9) is formed to be continuous with the wiring line (11). Izumi et al. does not disclose expressly a hydrogen barrier film entirely covering the capacitor upper electrode. Evans, Jr., Figure 10, discloses (col. 6, lines 40-44) a hydrogen barrier (255) entirely covering the platinum upper electrode (214) of a capacitor. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form a hydrogen barrier entirely covering the upper capacitor electrode of Izumi et al.. The motivation for doing so would have been prevent hydrogen from reaching the electrode and dielectric of the capacitor (col. 8, lines 22-26). Therefore, it would have been obvious to combine Evans, Jr. with Izumi et al. to obtain the invention as specified in claim 1.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al. in view of Evans, Jr. and further in view of Koyama. As to claim 2, Izumi et al. in view of Evans, Jr. discloses the device of claim 1, as described above. Izumi et al. in view of Evans, Jr. does not disclose expressly insulating sidewalls formed on respective side surfaces of the capacitor lower electrode and insulating film. Koyama, Figure 8, discloses (col. 3, lines 22-24) insulating sidewalls (6-2) formed on respective side surfaces of a capacitor lower electrode (13) and capacitor insulating film (10), and a capacitor upper electrode (7-2) formed over the capacitor insulating film and the sidewalls. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form sidewalls on the side surfaces of the capacitor of Izumi et al. in view of Evans, Jr.. The motivation for doing so would have been to dielectrically isolate the capacitor film and lower electrode from further layers formed over the device, as shown in Koyama, Figure 8. Therefore, it would have been obvious to combine Koyama with Izumi et al. in view of Evans, Jr. to obtain the invention as specified in claim 2.

As to claim 3, Koyama discloses (col. 4, lines 3-5) that the sidewalls are made of silicon oxide.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al. in view of Evans, Jr. and further in view of Sandhu et al.. As to claim 4, Izumi et al. in view of Evans, Jr. discloses the device of claim 1, as described above. Izumi et al. in view of Evans, Jr. does not disclose expressly a plurality of capacitor lower electrodes separated by an insulating film with the capacitor insulating film formed over the plurality of lower electrodes. Sandhu et al., Figure 3, discloses (col. 6,

Art Unit: 2826

lines 34-40) a plurality of capacitor lower electrodes formed on a protective insulating film (18), with an insulating film (66) formed between the plurality of capacitor lower electrodes, wherein the capacitor insulating film (50) is formed over the plurality of capacitor lower electrodes (44) and the insulating film (66). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form sidewalls on the side surfaces of the capacitor of Izumi et al. in view of Evans, Jr.. The motivation for doing so would have been to dielectrically isolate the capacitor film and lower electrode from further layers formed over the device, as shown in Koyama, Figure 8. Therefore, it would have been obvious to combine Sandhu et al. with Izumi et al. in view of Evans, Jr. to obtain the invention as specified in claim 4.

As to claim 5, Sandhu et al. discloses (col. 6, line 38) that the insulating film may be made of silicon oxide.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al. in view of Evans, Jr. and further in view of Graettinger et al.. Izumi et al. in view of Evans, Jr. discloses the device of claim 1, as described above. Izumi et al. in view of Evans, Jr. does not disclose expressly each of the first and second contact plugs made from polysilicon or tungsten. Graettinger et al., Figure 1, discloses (col. 3, line 57) contact plugs formed between a transistor diffusion region and a capacitor lower electrode from polysilicon. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the contact plugs of the first and second capacitors of Izumi et al. in view of Evans, Jr. from polysilicon. The motivation for doing so would have been to form a conductive path to the bottom electrode. Therefore, it would have been obvious to combine Graettinger et al. with Izumi et al. in view of Evans, Jr. to obtain the invention as specified in claim 6.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Izumi et al. in view of Evans, Jr. and further in view of Jones, Jr.. Izumi et al. in view of Evans, Jr. discloses the device of claim 1, as described above. Izumi et al. in view of Evans, Jr. does not disclose expressly the capacitor insulating film formed from one of the claimed materials. Jones, Jr., Figure 14, discloses (col. 4, lines 15-17) the capacitor insulating film formed from lead zirconate titanate. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the capacitor insulating film of Izumi et al. in view of Evans, Jr. from lead zirconate titanate. The motivation for doing so would have been to enable

Art Unit: 2826

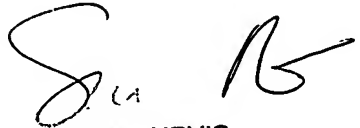
the conversion of the material to its perovskite phase (Jones, Jr., col. 4, lines 19-20). Therefore, it would have been obvious to combine Jones, Jr. with Izumi et al. in view of Evans, Jr. to obtain the invention as specified in claim 7.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SRW
March 26, 2007


SUE A. PURVIS
SUPERVISORY PATENT EXAMINER